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A high-efficiency Class E inverter – computer model, laboratory measurements and SPICE simulation

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Abstract. The paper presents the theoretical background, computer model, laboratory measurements and SPICE simulation results of a 323 W, 1 MHz Class E inverter operating with an efficiency of 97%. The inverter is built around a CoolMOS transistor from Infineon Technologies. The transistor belongs to a new generation of high quality, optimized for low conduction losses and high speed switching power MOSFET-s. The presented computer model of Class E inverter is based on a state-space description and allows computing the inverter parameters for the optimum operation. Its validity has been confirmed experimentally. The SPICE simulation of the inverter has been also carried out in order to obtain better agreement between measurement and calculation results.

Key words: Class E inverter, ZVS, high-efficiency, high-frequency, simulation.

1. Introduction

There are a large variety of industrial, scientific and medical processes that require reliable, low cost, high-frequency supply sources. Such applications include induction and dielectric heating, induction generation of plasma, power supplies for lasers, medical implanted systems and glass coating, transmitters for communication and dc/dc converters. Class E inverters meet these requirements. They have high-efficiency, high density of power processing, high reliability, simplicity, excellent designability, and low cost and size [1–4].

The purpose of this paper is to design, build and examine a high-efficiency Class E inverter using a CoolMOS transistor, verify its computer model, and finally, present SPICE analysis of this inverter.

CoolMOS is an example of new trends in technology of semiconductor devices. It is applicable for high voltage power MOSFET-s and implements a compensation structure in the vertical drift region of a MOSFET in order to improve its on-resistance [5]. The transistor chip area for the same on-resistance in comparison with standard MOSFET technologies is significantly reduced. For example, a SPP20N65C3 CoolMOS transistor (650 V, 21 A, 0.19 Ω) and a standard IRFP460 MOSFET transistor (500 V, 20 A, 0.27 Ω) have TO-220 (15 mm × 10 mm) and TO-247 (20 mm × 15 mm) packages, respectively. As a result, CoolMOS transistors not only have lower on-resistances, but also surpass their competitors in dynamic performance. This type of transistors seem to be particularly suitable for use in Class E inverters operating in the MHz range, however, it is hard to find any example of their applications in such inverters.

The literature is full of various models and methods for calculating parameters of Class E inverters. They neglect or take into account a transistor on-resistance (e.g. [1,4] or [6]), finite dc-feed inductance (e.g. [1,4] or [7]) and finite quality factor of the load network (e.g. [1,4] or [8]), but most of them are complicated and unclear. The proposed here model with nonzero transistor on-resistance, finite dc-feed inductance and finite quality factor is very easy to form and effective in computing by means of built-in functions of MATLAB software. Its validity has been confirmed experimentally. Such models can be prepared for other circuits.

A SPICE analysis of circuits is very useful in designing and optimizing their performance. The results obtained in this way are more accurate than those found by means of simplified models used in the design stage. This is because more transistor and circuit parameters can be taken into account. On the other hand, such analysis can only be performed for a specified case. Selected results of the Class E inverter simulation are presented in the last part of the paper.

2. Principle of operation

A Class E inverter is a well-known resonant converter that can operate at frequencies from hundreds of kHz to tens of MHz and power levels from watts to kilowatts with high-efficiency, e.g. [2, 9-11]. Its basic circuit is shown in Fig. 1. It consists of a choke inductor L_1, a shunt capacitor C_1, a series resonant circuit $C_2 - L_2$, a load resistor R, and a transistor Tr. Note that the shunt capacitance C_1 includes the output transistor capacitance. The transistor Tr is usually switched periodically at a duty cycle of 0.5. The proper choice of circuit parameters guarantees the transistor Tr is switched on for ZVS (zero-voltage switching) and ZdVS (zero-voltage slope switching) conditions that determine the optimum operation of Class E inverter (Fig. 2). The voltage and current waveforms of Fig. 2 are normalized to the dc supply voltage U and the average value I of the supply current i, respectively, and

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the time axis is normalized to the switching period T. During the off-interval of the transistor, the current i_T remains at zero while the voltage u_T increases to a maximum of 3.6 times the dc voltage U. At the end of the off-interval, when the voltage u_T has decreased to zero, the transistor is switched on and the current i_T increases toward a maximum of 2.9 times the dc current I. At the end of the on-interval, the transistor is switched off and the current i_T drops to zero before the voltage u_T begins to rise. During switching transitions, both transistor voltage and current have zero crossover values and, as a result, the only power losses remaining are the conduction losses. Efficiencies of Class E inverters can significantly exceed 90%. Increased efficiency not only means lower input power, but also less heat dissipation in the transistor.

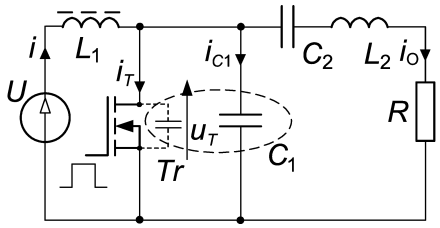

Fig. 1. Class E inverter circuit

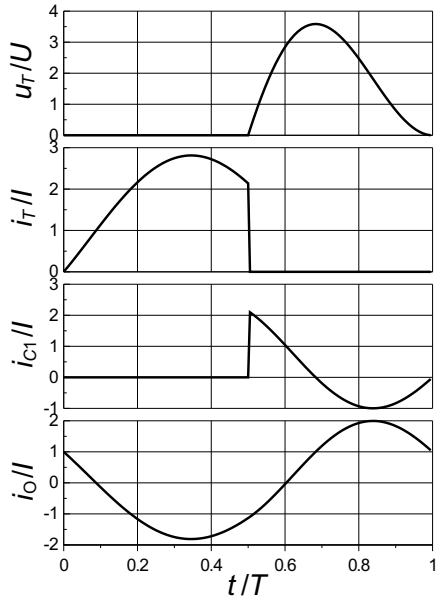

Fig. 2. Class E inverter waveforms (u_T – transistor voltage, i_T – transistor current, i_{C1} – capacitor current, and i_O – output current)

3. Class E inverter model

An inverter model is based on a state-space description of Class E inverter [12]. First, a steady-state solution is obtained. Next, the soft-switching conditions (ZVS and ZdVS) at the instant the transistor is switched on are introduced. Finally, numerical calculations are carried out to find the inverter parameters for the optimum operation. The main points of this procedure are presented below and a listing of the program in MATLAB is given in the appendix.

The following assumptions were adopted for the Class E inverter model: 1) the transistor acts as a switch with resistance of $R_{T\mathrm{on}}$ for the on-interval, infinite resistance for the off-interval, and zero switching times; 2) the shunt capacitance C_1 is independent of switch voltage and includes the transistor output capacitance; and 3) all passive elements are ideal and time invariant. The switch is driven at any frequency f and at any duty cycle D, where the duty cycle is defined as switch on-time divided by the switching period ($T = 1/f$).

The circuits of Fig. 3 can be described by a normalized set of state equations of the form:

$$\frac{\mathrm{d}\mathbf{x}^\bullet}{\mathrm{d}\theta} = \mathbf{A}^\bullet \mathbf{x}^\bullet + \mathbf{B}^\bullet, \tag{1}$$

where $\mathbf{x}^\bullet = [x_1^\bullet, x_2^\bullet, x_3^\bullet, x_4^\bullet]^T$ – state vector, $x_{1,2}^\bullet = \frac{x_{1,2}}{U}$ – normalized voltages, $x_{3,4}^\bullet = \frac{x_{3,4}}{U/R}$ – normalized currents, $\theta = 2\pi f t = \omega t$, $\mathbf{A}^\bullet = \begin{bmatrix} a_{11}^\bullet & 0 & X_{C1}^\bullet & -X_{C1}^\bullet \\ 0 & 0 & 0 & X_{C2}^\bullet \\ -1/X_{L1}^\bullet & 0 & 0 & 0 \\ 1/X_{L2}^\bullet & -1/X_{L2}^\bullet & 0 & -1/X_{L2}^\bullet \end{bmatrix}$, $X_{C1}^\bullet = 1/(\omega C_1 R)$, $X_{C2}^\bullet = 1/(\omega C_2 R)$, $X_{L1}^\bullet = \omega L_1/R$, $X_{L2}^\bullet = \omega L_2/R$ – normalized reactances, $\mathbf{B}^\bullet = [0, 0, 1/X_{L1}^\bullet, 0]^T$. Denoting the matrix $\mathbf{A}^\bullet$ for the on-interval ($a_{11}^\bullet = -X_{C1}^\bullet/R_{T\mathrm{on}}^\bullet$, $R_{T\mathrm{on}}^\bullet = R_{T\mathrm{on}}/R$ – normalized resistance) by $\mathbf{A}_{on}^\bullet$ and for the off-interval ($a_{11}^\bullet = 0$) by $\mathbf{A}_{off}^\bullet$, in the case the matrices $\mathbf{A}_{on}^\bullet$ and $\mathbf{A}_{off}^\bullet$ are nonsingular we can write the solution of (1) in the following two parts [12]:

$$\mathbf{x}_{on}^\bullet(\theta) = \mathbf{x}^\bullet(\theta)|_{\mathbf{A}^\bullet = \mathbf{A}_{on}^\bullet} = \mathrm{expm}(\mathbf{A}_{on}^\bullet \theta)\mathbf{x}_{on}^\bullet(0) + {\mathbf{A}_{on}^\bullet}^{-1}(\mathrm{expm}(\mathbf{A}_{on}^\bullet \theta) - \mathbf{I})\mathbf{B}^\bullet, \tag{2a}$$

$$\mathbf{x}_{off}^\bullet(\theta) = \mathbf{x}^\bullet(\theta)|_{\mathbf{A}^\bullet = \mathbf{A}_{off}^\bullet} = \mathrm{expm}(\mathbf{A}_{off}^\bullet \theta)\mathbf{x}_{off}^\bullet(0) + {\mathbf{A}_{off}^\bullet}^{-1}(\mathrm{expm}(\mathbf{A}_{off}^\bullet \theta) - \mathbf{I})\mathbf{B}^\bullet, \tag{2b}$$

where $\mathrm{expm}(\mathbf{A}^\bullet\theta)$ is the matrix exponential of $\mathbf{A}^\bullet\theta$, $\mathbf{x}_{on}^\bullet(0)$ and $\mathbf{x}_{off}^\bullet(0)$ are initial conditions for the on- and off-interval, respectively, and $\mathbf{I}$ is the 4-by-4 identity matrix. Using the continuity conditions we obtain:

$$\mathbf{x}_{on}^\bullet(\theta = 2\pi D) = \mathbf{x}_{off}^\bullet(0), \tag{3a}$$

$$\mathbf{x}_{off}^\bullet(\theta = 2\pi(1-D)) = \mathbf{x}_{on}^\bullet(0), \tag{3b}$$

and finally, the initial conditions can be calculated as follows:

$$\begin{bmatrix} \mathbf{x}_{on}^\bullet(0) \\ \mathbf{x}_{off}^\bullet(0) \end{bmatrix} = \begin{bmatrix} -\mathrm{expm}(\mathbf{A}_{on}^\bullet 2\pi D) & \mathbf{I} \\ \mathbf{I} & -\mathrm{expm}(\mathbf{A}_{off}^\bullet 2\pi(1-D)) \end{bmatrix}^{-1} \cdot \begin{bmatrix} {\mathbf{A}_{on}^\bullet}^{-1}(\mathrm{expm}(\mathbf{A}_{on}^\bullet 2\pi D) - \mathbf{I}) \\ {\mathbf{A}_{off}^\bullet}^{-1}(\mathrm{expm}(\mathbf{A}_{off}^\bullet 2\pi(1-D)) - \mathbf{I}) \end{bmatrix} \mathbf{B}^\bullet. \tag{4}$$

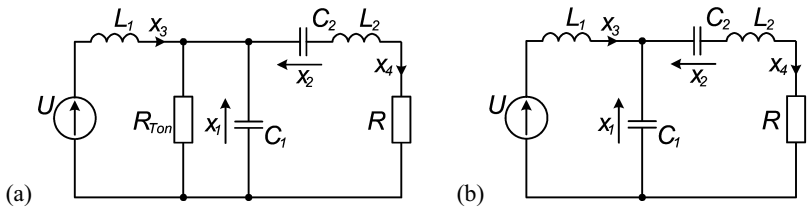

Fig. 3. Equivalent circuits of Class E inverter: (a) switch on-interval, (b) switch off-interval

Once (4) is given the steady-state solution is obtained from (2). Next, the steady-state solution is completed by adding the soft-switching conditions. The ZVS condition demands that the switch voltage at the instant the switch is turned on should be zero:

$$x^{\bullet}_{on1}(0) = 0 \tag{5}$$

The ZdVS condition ensures that the switch current starts from zero and it is given by:

$$x^{\bullet}_{on3}(0) - x^{\bullet}_{on4}(0) = 0 \tag{6}$$

Equations (2) and (4) form the Class E inverter model for steady-state. A computer program in MATLAB (see appendix) is used to find solutions to Eqs. (4), (5), and (6) for different input data, ensuring the optimum operation of the Class E inverter. The calculation procedure can be summarized in the following steps:

1. Setting values for input data: D, $R^{\bullet}_{T\mathrm{on}}$, $X^{\bullet}_{L1}$, $X^{\bullet}_{L2}$.
2. Specifying initial values for: $X^{\bullet}_{C1}$, $X^{\bullet}_{C2}$ (taken from the previous or simplified analysis).
3. Finding the solution to (4), (5), and (6) by changing $X^{\bullet}_{C1}$, $X^{\bullet}_{C2}$.
4. Saving the results.

4. Class E inverter design

A design procedure is explained with an example circuit of Class E inverter. Selected results of the use of the program from the appendix are given in Table I. They were calculated for different values of $R^{\bullet}_{T\mathrm{on}}$, $X^{\bullet}_{L1}$, $X^{\bullet}_{L2}$ and the constant duty cycle $D = 0.5$. There is a lower limit on the minimum value of $X^{\bullet}_{L2}$ for which the shunt capacitor C_1 is a dc blocking capacitor ($X^{\bullet}_{C2} = 0$). The normalized transistor on-resistance $R^{\bullet}_{T\mathrm{on}}$ impacts on the inverter efficiency and affects to some extent other inverter parameters. Table 1 and the equations given in (1) and (7) enable the calculation of approximate values of the inverter parameters. More accurate design can be obtained using the actual values of $R^{\bullet}_{T\mathrm{on}}$, $X^{\bullet}_{L1}$, $X^{\bullet}_{L2}$, and D (Section 5).

The specifications of the example circuit are: the operating frequency $f = 1$ MHz, the transistor peak voltage $U_{T\mathrm{m}} = 455$ V, the transistor rms current $I_{T\mathrm{rms}} = 5$ A, and the parameters marked in bold style (Table I). The values of $X^{\bullet}_{L1}$ and $X^{\bullet}_{L2}$ were chosen to reduce losses and size of the inductors L_1 and L_2. First, the load resistance R is calculated as:

$$R = \frac{U_{T\mathrm{m}}}{U^{\bullet}_{T\mathrm{m}}} \frac{I^{\bullet}_{T\mathrm{rsm}}}{I_{T\mathrm{rsm}}} \frac{1}{R^{\bullet}_{\mathrm{dc}}} = \frac{455}{3.61} \frac{1.53}{5} \frac{1}{1.89} = 20.4\ \Omega, \tag{7}$$

next, the remaining values of components are calculated: $L_1 = RX^{\bullet}_{L1}/\omega = 20.4 \cdot 100/(2\pi \cdot 10^6) = 325$ μH, $L_2 = 16.2$ μH, $C_1 = 1/X^{\bullet}_{C1}/\omega/R = 1/4.65/(2\pi \cdot 10^6)/20.4 = 1.68$ nF, $C_2 = 2.09$ nF, and finally, the supply parameters are: $U = U_{T\mathrm{m}}/U^{\bullet}_{T\mathrm{m}} = 455/3.61 = 126$ V, $I = I_{T\mathrm{rms}}/I^{\bullet}_{T\mathrm{rms}} = 5/1.53 = 3.27$ A, $P = U \cdot I = 126 \cdot 3.27 = 412$ W.

Table 1
Parameters of Class E inverter for $D = 0.5$

$R^{\bullet}_{T\mathrm{on}} = 0.001$							$R^{\bullet}_{T\mathrm{on}} = 0.05$							
$X^{\bullet}_{L1}$	$X^{\bullet}_{L2}$	$X^{\bullet}_{C1}$	$X^{\bullet}_{C2}$	$U^{\bullet}_{T\mathrm{m}}$	$I^{\bullet}_{T\mathrm{rms}}$	$R^{\bullet}_{\mathrm{dc}}$	$X^{\bullet}_{L1}$	$X^{\bullet}_{L2}$	$X^{\bullet}_{C1}$	$X^{\bullet}_{C2}$	$U^{\bullet}_{T\mathrm{m}}$	$I^{\bullet}_{T\mathrm{rms}}$	$R^{\bullet}_{\mathrm{dc}}$	η
1000	10	5.04	8.79	3.59	1.53	1.82	1000	10	5.18	8.75	3.49	1.54	1.95	94.0
1000	7.5	4.94	6.27	3.60	1.53	1.85	1000	7.5	5.07	6.23	3.50	1.53	1.99	94.1
1000	5	4.77	3.72	3.61	1.53	1.93	1000	5	4.89	3.67	3.52	1.53	2.08	94.3
1000	2.5	4.53	0.99	3.68	1.53	2.29	1000	2.5	4.62	0.94	3.59	1.54	2.46	95.2
1000	1.79	4.58	0	3.73	1.55	2.77	1000	1.83	4.66	0	3.65	1.55	2.92	95.9
100	10	4.92	8.81	3.59	1.53	1.78	100	10	5.05	8.77	3.49	1.54	1.92	93.9
100	7.5	4.82	6.29	3.60	1.53	1.82	100	7.5	4.95	6.25	3.50	1.53	1.95	94.0
100	**5**	**4.65**	**3.74**	**3.61**	**1.53**	**1.89**	100	5	4.77	3.69	3.52	1.53	2.03	94.2
100	2.5	4.40	1.02	3.67	1.53	2.22	100	2.5	4.50	0.97	3.59	1.53	2.39	95.1
100	1.75	4.44	0	3.73	1.55	2.69	100	1.79	4.52	0	3.65	1.55	2.84	95.8
10	10	3.98	8.97	3.60	1.53	1.52	10	10	4.08	8.93	3.48	1.53	1.64	92.8
10	7.5	3.91	6.46	3.60	1.53	1.54	10	7.5	4.00	6.41	3.48	1.53	1.66	93.0
10	5	3.78	3.92	3.62	1.53	1.58	10	5	3.86	3.87	3.50	1.53	1.71	93.2
10	2.5	3.54	1.27	3.67	1.53	1.77	10	2.5	3.61	1.22	3.56	1.53	1.91	93.9
10	1.50	3.47	0	3.74	1.55	2.14	10	1.54	3.53	0	3.64	1.55	2.27	94.7

where $U^{\bullet}_{T\mathrm{m}} = U_{T\mathrm{m}}/U$ – normalized transistor peak voltage, $I^{\bullet}_{T\mathrm{rms}} = I_{T\mathrm{rms}}/I$ – normalized transistor rms current, $R^{\bullet}_{\mathrm{dc}} = U/(I \cdot R)$ – normalized inverter input resistance, and η – inverter efficiency for $R^{\bullet}_{T\mathrm{on}} = 0.05$.

5. Experimental results

The computer model has been verified experimentally in the Class E inverter circuit of Fig. 4. The photograph of the laboratory setup is shown in Fig. 5. The preliminary design of the inverter is given in Section 4.

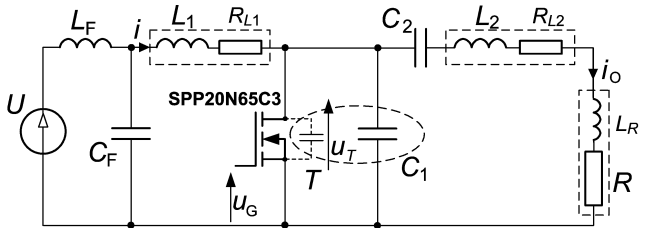

Fig. 4. Circuit diagram of Class E inverter

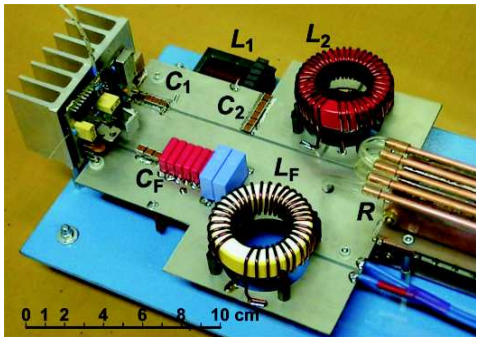

Fig. 5. General view of fabricated Class E inverter

A SPP20N65C3 CoolMOS transistor (650 V, 21 A) from Infineon Technologies was used as the switching device. Its gate-driver circuitry enables the duty cycle D and frequency f to be adjusted. The transistor is mounted directly to a backside aluminium heatsink, using it as the drain connection to the circuit board. The dc supply passes through the input filter (Fig. 4, 5), the choke $L_{\rm F}$ (0.45 mH) and the bypass capacitor $C_{\rm F}$ (2.5 μF). All components of the inverter were measured using a HP4294A Impedance Analyzer. The following results were obtained: $L_1 = 270$ μH (ferrite core inductor with air gap), $R_{L1} = 40$ mΩ (dc parasitic resistance), $C_1 = 1.72$ nF (silver mica capacitors and transistor output capacitance), $C_2 = 2.00$ nF (silver mica capacitors), $L_2 = 16.8$ μH (iron powder core inductor), $R_{L2} = 0.29$ Ω (parasitic resistance at 1 MHz), and $R = 20.04$ Ω (resistance of 60 power film resistors connected in series-parallel and mounted on water cooled heatsink), $L_R = 7.3$ nH (parasitic inductance). Power losses of all capacitors were negligible.

A calibrated Tektronix TDS3034B digital oscilloscope with voltage (P6139A) and current (TCP202, P6022) probes was used for recording voltage and current waveforms. In order to obtain accurate readings of transistor power losses a comparative thermal method was used. First, a thermocouple was attached to the transistor case. Next, dc power was supplied to the transistor with its gate-source connected to +12 V. In thermal steady-state, the transistor voltage U_T and the transistor current I_T were measured. At the same time, the temperature rise ΔT was recorded using a National Instruments PCI-6052 multi-function DAQ card. Finally, the power losses $P_T (P_T = U_T \cdot I_T)$ dissipated in the transistor and the transistor on-resistance $R_{T\rm on}$ ($R_{T\rm on} = U_T/I_T$) were calculated. The results are plotted in Fig. 6.

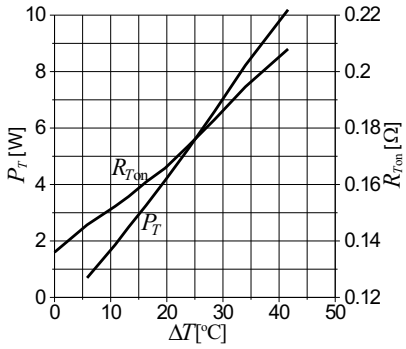

Fig. 6. Plots of P_T and $R_{T\rm on}$ versus ΔT for the ambient temperature of 25°C

The oscilloscope waveforms of Fig. 7 illustrate the optimum operation of the Class E inverter. They were recorded for the supply voltage $U = 129.0$ V, the supply current $I = 2.58$ A, the input power $P = 332.8$ W, the duty cycle $D = 0.47$, and the operating frequency $f = 1.024$ MHz. The temperature rise ΔT was 23.6°C. The transistor losses P_T and the transistor on-resistance $R_{T\rm on}$ were 5.2 W and 0.174 Ω (Fig. 6), respectively, resulting in the drain efficiency η_D ($\eta_D = (1 - P_T/P) \cdot 100\%$) of 98.4%. The transistor peak voltage $U_{T\rm m}$ was 455.2 V Fig. 7(a). The output power P_O was calculated using the supply current I and rms output current $I_{O\rm rms}$ Fig. 7(b) as:

$$P_{\rm O} = P - P_T - I^2 R_{L1} - I_{\rm Orms}^2 R_{L2} = 332.8 - 5.2 - 2.58^2 0.04 - 4^2 0.29 = 322.7 \text{ W}. \quad (8)$$

The total efficiency η ($\eta = P_O/P \cdot 100\%$) was 97.0%. As a result of the applied method, the standard uncertainties of the calculated output power P_O and efficiency η (η_D) were low, respectively 1.5 W and 0.5%.

In order to confirm the validity of the Class E inverter model from section 3 the following comparison was carried out. For the parameters of the laboratory inverter ($D = 0.47$, $f = 1.024$ MHz, $L_1 = 270$ μH, $L_2 = 16.8$ μH, $R_{T\rm on} = 0.174$ Ω, $R = 20.04 + 0.29 = 20.33$ Ω, $U = 129$ V) once more the design procedure was applied. Its results are given in Table 2, as theoretical ones, and they are compared with the measurements. The experimental and theoretical results are in good agreement, with the exception of the transistor losses P_T. These losses equal the total power dissipated in the transistor while in the model they are only calculated as the power associated with the transistor on-resistance. Furthermore, the on-resistance of the applied transistor is relatively low and, as a result, the ratio of the power losses associated with switching off the transistor to the conduction losses can be higher than usually. The discrepancy between the theoretical and experimental results can also be caused by the assumption in the model that the shunt capacitance C_1 is linear. Therefore, this problem is examined further in Section 6.

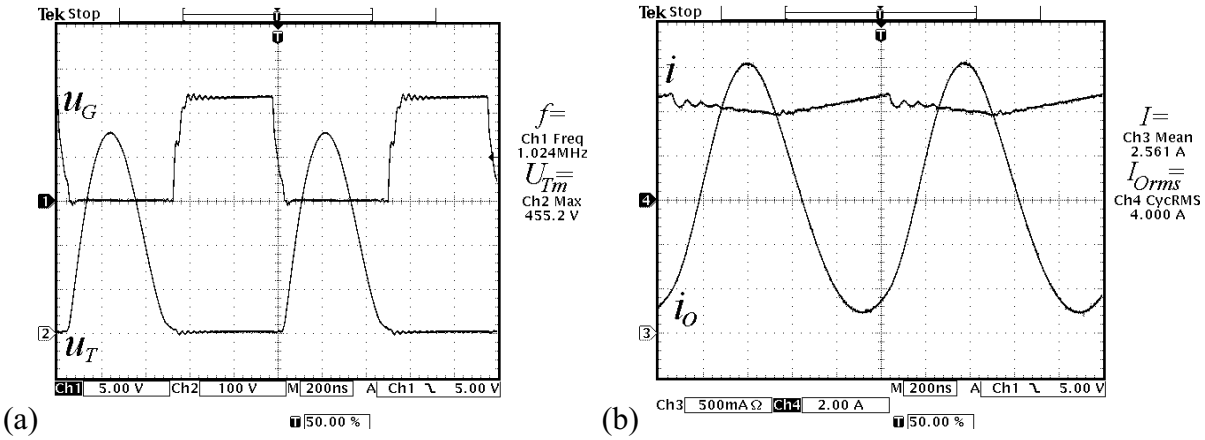

Fig. 7. Waveforms of gate-source voltage u_G and transistor voltage u_T (a), supply current i and output current i_O (b)

Table 2
Theoretical and experimental parameters of Class E inverter

Parameter	Theoretical (*theo*)	Experimental (*expe*)	Difference* (*diff*)
C_1 [nF]	1.77	1.72 (estimated)	−2.9
C_2 [nF]	1.96	2.00	2.0
I [A]	2.74	2.58	−6.2
$I_{O\mathrm{rms}}$ [A]	4.15	4.00	−3.8
$U_{T\mathrm{m}}$ [V]	439	455	3.5
P_T [W]	3.3	5.2	37

* *diff* = (*expe* − *teo*)/*expe* · 100%

It should be noticed that in the case of using a simplified model for calculating the Class E inverter parameters (i.e. $D = 0.5$, $R_{T\mathrm{on}} \approx 0$, $L_1 >> L_2$, $X^{\bullet}_{L2} > 10$), the differences analogous to those given in Table 2 would be higher. For example, the capacitances C_1 and C_2 calculated by means of the formulas presented in [4] are as follows: 1.40 nF and 1.84 nF.

6. Spice simulation

A SPP20N65C3 CoolMOS model provided by Infineon Technologies [5] was used in the SPICE simulation of the Class E inverter. The rest of the necessary parameters (Fig. 8) were fixed in accordance with the laboratory setup. Only the value of the capacitance C_1 was carefully adjusted to 1.47 nF in order to ensure the optimum operation of the inverter.

The SPICE simulation results for steady-state are shown in Fig. 9. It is seen that they are very close to the measurements presented in Fig. 7. Their quantitative comparison shows better agreement than that detailed previously in Table 2. The simulation results are as follows: $I = 2.67$ A with relative difference (*diff*) of -3.5% between the experimental and simulation values, $I_{O\mathrm{rms}} = 4.09$ A (-2.3%), $U_{T\mathrm{m}} = 462$ V (-1.5%), and $P_T = 4.7$ W (10%).

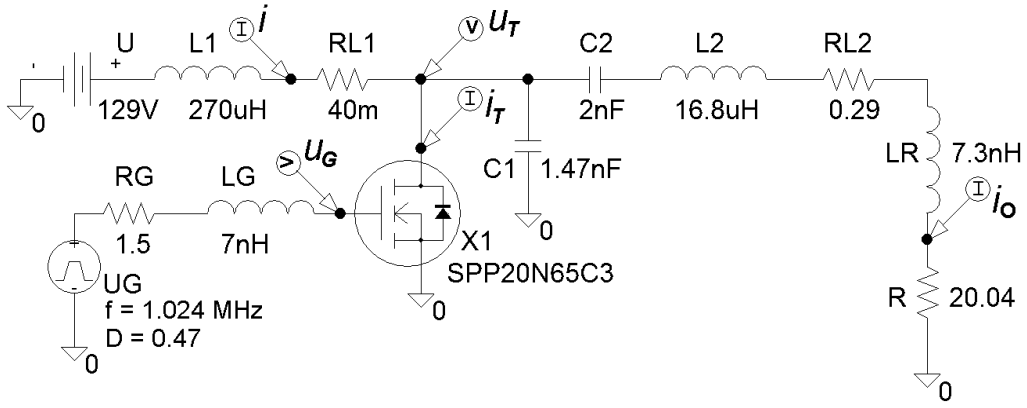

Fig. 8. Class E inverter model for SPICE simulation

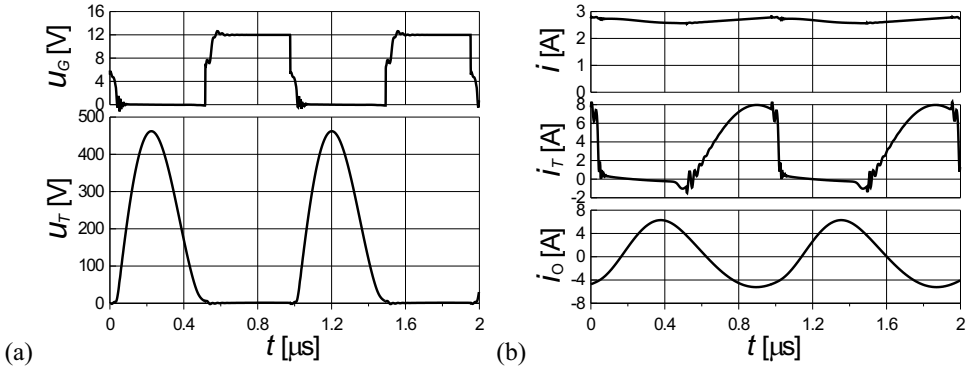

Fig. 9. Simulated waveforms of Class E inverter model:
a) gate-source voltage u_G and transistor voltage u_T, b) supply current i, transistor current i_T, and output current i_o

7. Conclusions

A state-space technique has been used to provide the computer model of Class E inverter, including a transistor on-resistance, finite dc-feed inductance and finite quality factor of the load network. The model allows the designer to perform the simple and efficient design of the Class E inverter in the topology shown in Fig. 1. The presented procedure can be easy implemented to other circuits, for example Class D and DE inverters.

A high-efficiency 1 MHz Class E inverter using a SPP20N65C3 CoolMOS transistor have been successfully designed, fabricated and tested. Optimized static (low on-resistance) and dynamic (low gate charge) performance of the applied transistor enable the inverter to produce 322.7 W output power with the drain efficiency of 98.4% and the total efficiency of 97%.

Experimental measurements have confirmed the validity of the Class E inverter model. A yet better agreement has been obtained between the measurement and SPICE simulation results. This is due to taking into account the effect of parasitic parameters and the use of the transistor model offered by the producer.

Appendix

The following simplified denotations rT, D, xL1, xL2, xC1, xC2, Aon, Aoff, B, xon, xoff, ITav, ITrms, UTm, rdc, eff, are introduced instead of $R^{\bullet}_{T\mathrm{on}}$, D, $X^{\bullet}_{L1}$, $X^{\bullet}_{L2}$, $X^{\bullet}_{C1}$, $X^{\bullet}_{C2}$, $\mathbf{A}^{\bullet}_{on}$, $\mathbf{A}^{\bullet}_{off}$, $\mathbf{B}^{\bullet}$, $\mathbf{x}^{\bullet}_{on}$, $\mathbf{x}^{\bullet}_{off}$, $I^{\bullet}$, $I^{\bullet}_{T\mathrm{rms}}$, $U^{\bullet}_{T\mathrm{m}}$, $R^{\bullet}_{\mathrm{dc}}$, η, respectively.

The following is a listing of the main program *start*:

```
% This M-file calculates the Class E inverter parameters for
% the optimum operation.
% defining global variables
global rT xL1 xL2 D Aon Aoff B xon xoff par;
% setting values for input and initial data
D=0.5; rT=0.05; xL1=1000; xL2=10; xC1=5; xC2=8.8;
% calculating xC1 and xC2 for the optimum operation using
% the built-in function fsolve, which solves the system of
% nonlinear equations defined by the user function soft
xC = fsolve ('soft',[xC1; xC2]);
xC1 = xC(1); xC2 = xC(2);
% calculating state matrices Aon, Aoff, B and vectors xon,
% xoff using the user function sol
[x, Aon, Aoff, B] = sol (xC1, xC2);
xon=x([1:4]); xoff=x([5:8]);
% calculating ITav, rdc, ITrms, Utm, eff using the built-in
% functions quadl (numerical integration), fminbnd (scalar
% bounded nonlinear function minimization), and the user
% function fun
par=1; ITav = quadl('fun', 0, 2*pi*D)/(2*pi); rdc = 1/ITav;
par=2; ITrms = sqrt(quadl('fun', 0, 2*pi*D)/(2*pi));
ITrms = ITrms*rdc;
par=4; arg = fminbnd('fun', 0, 2*pi*(1-D));
par=3; UTm = fun(arg);
eff = 1-rT*ITrms^2/rdc;
% plotting the switch voltage u_T using the user function fun
par=3; figure(1); wek = 0:2*pi*(1-D)/100:2*pi*(1-D);
plot(wek, fun(wek));
% plotting the switch current i_T using the user function fun
par=1; figure(2); wek = 0:2*pi*D/100:2*pi*D;
plot(wek, fun(wek)):
```

The following is a listing of the function *soft*:

```
% This function defines the soft-switching conditions.
function q = soft (xC);
% calculating the initial conditions x using the function sol
x = sol (xC(1), xC(2));
q(1) = x(5); % ZVS condition
q(2) = x(7)-x(8); % ZdVS condition
```

The following is a listing of the function *sol*:

```
% This function calculates the initial conditions x and
% the state matrices [x, Aon, Aoff, B] = sol (xC1, xC2);
global rT xL1 xL2 D;
Aon = [-xC1/rT 0 xC1 -xC1; 0 0 0 xC2; -1/xL1 0 0 0; 1/xL2
-1/xL2 0 -1/xL2];
Aoff = Aon; Aoff(1,1) = 0; B = [0 0 1/xL1 0]';
x = [-expm(Aon*D*2*pi) eye(4); eye(4) -expm(Aoff*(1-D)*
2*pi)]\ [Aon\(expm(Aon*D*2*pi)-eye(4)); Aoff\(expm(Aoff*
(1-D)*2*pi)-eye(4))]*B;
```

The following is a listing of the function *fun*:

```
function q = fun (z);
global Aon Aoff B rT xon xoff par;
% defining the function of the switch current for the on-
% interval
if par==1; wym = length(z);
for i=1:1:wym;
x = expm(Aon*z(i))*xon+Aon\(expm(Aon*z(i))-eye(4))*B;
q(i) = x(1)/rT;
end; end;
% defining the function of the square switch current for the
% on-interval
if par==2; wym = length(z);
for i=1:1:wym;
x = expm(Aon*z(i))*xon+Aon\(expm(Aon*z(i))-eye(4))*B;
q(i) = (x(1)/rT)^2;
end; end;
% defining the function of the switch voltage for the off-
% interval
if par==3; wym = length(z);
for i=1:1:wym;
x = expm(Aoff*z(i))*xoff+Aoff\(expm(Aoff*z(i))-eye(4))*B;
q(i) = x(1);
end; end;
% defining the function of the opposite switch voltage for the
% off-interval
if par==4; wym = length(z);
for i=1:1:wym;
x = expm(Aoff*z(i))*xoff+Aoff\(expm(Aoff*z(i))-eye(4))*B;
q(i) = -1*x(1);
end; end;
```

REFERENCES

[1] N.O. Sokal and A.D. Sokal, "Class E – a new class of high-efficiency tuned single-ended switching power amplifiers", *IEEE J. Solid-State Circuits* SC-10 (3), 168–176 (1975).

[2] N.O. Sokal, "Class-E RF power amplifiers", *QEX Communications Quarterly* 204, 9–20 (2001).

[3] F.H. Raab, "Idealized operation of the Class E tuned power amplifier", *IEEE Trans. Circuits and Systems* CAS-24 (12), 725–735 (1977).

[4] M. Kazimierczuk, "Theory of high-frequency Class E power amplifier", *Thesis on Electrotechnics* 25 (4), 957–986 (1979).

[5] http://www.infineon.com.

[6] C.P. Avratoglou, N.C. Voulgaris, and F.I. Ioannidou, "Analysis and design of a generalised Class E tuned power amplifier", *IEEE Trans. Circuits and Systems* 36 (8), 1068–1079 (1989).

[7] R.E. Zulinski and J.W. Steadman, "Class E power amplifiers and frequency multipliers with finite DC-feed inductance", *IEEE Trans. Circuits and Systems* 34 (9), 1074–1087 (1987).

[8] M.K. Kazimierczuk and K. Puczko, "Class E tuned power amplifier with antiparallel diode or series diode at switch, with any loaded Q and switch duty cycle", *IEEE Trans. Circuits and Systems* 36 (9), 1201–1209 (1989).

[9] G.J. Krausse, "1kW Class-E 13.56MHz single device RF generator for industrial appli cations", *Application Note -9300-0001, Directed Energy, Inc.*, www.ixysrf.com.

[10] Z. Kaczmarczyk, "An analysis of high frequency power electronic Class E inverter", *Ph.D. Thesis*, Silesian University of Technology, Gliwice, 1996.

[11] Z. Kaczmarczyk, "Improving properties of high-frequency Class E inverters", *Archives of Electrical Engineering* LIII (4), 449–459 (2004).

[12] L.O. Chua and P.M. Lin, *Computer-aided Analysis of Electronic Circuits*, WNT, Warszawa, 1981.